Claims

1. An image signal processing circuit that controls an amount of exposure for each of first and second solid state imaging devices that operate in a time-division manner, the processing circuit comprising:

an exposure control section that generates first and second exposure data, each of which indicates an amount of exposure for one of the first and second solid state imaging devices, so that a value of each of first and second image signals output from the first and second solid state imaging devices falls within predetermined limits, wherein the exposure control section includes:

a first memory section that stores the first exposure data; and

a second memory section that stores the second exposure data.

2. An image signal processing circuit according to claim 1, wherein, during a period when one of the first and second solid state imaging devices is operating, a value of one of the first and second exposure data is successively updated in accordance with an image signal obtained from the operating solid state imaging device, and a value of another one of the first and second exposure data is held without being updated.

3. An image signal processing circuit according to claim 2, wherein, when operation is switched between the first and second solid state imaging devices, the value of the exposure data that is held during the period of suspension of operation is used as an initial value to start operation.

4. An image signal processing circuit according to claim 2, wherein, when operation is switched between the first and second solid state imaging devices, the values of the first and second exposure data input immediately before a time of switching of operation are held for a predetermined period from the time of switching of operation.

5. An image signal processing circuit that corrects white balance by applying predetermined gains to each of first and second image signals output from first and second solid state imaging devices that operate in a time-division manner, the processing circuit comprising:

a white balance processing section that generates first and second gain data, each of which indicates amount of gain for one of the first and second image signals, wherein the white balance processing section includes:

a first memory section that stores the first gain data; and

a second memory section that stores the second gain data.

6. An image signal processing circuit according to claim 5, wherein, during a period when one of the first and second solid state imaging devices is operating, a value of one of the first and second gain data is successively updated in accordance with an image signal obtained from the operating solid state imaging device, and a value of another one of the first and second gain data is held without being updated.

7. An image signal processing circuit according to claim 6, wherein, when operation is switched between the first and second solid state imaging devices, the value of the gain data that is held during the period of suspension of operation is used as an initial value to start operation.

8. An image signal processing circuit according to claim 6, wherein, when operation is switched between the first and second solid state imaging devices, the values of the first and second gain data input immediately before time of switching of operation are held for a predetermined period from the time of switching of operation.

9. An imaging unit, comprising:

a first solid state imaging device having a plurality of light receiving pixels that accumulate information charges generated in response to a first picture of a subject;

a first driving circuit that drives the first solid state

imaging device to obtain a first image signal;

a second solid state imaging device having a plurality of light receiving pixels that accumulate information charges generated in response to a second picture of the subject;

a second driving circuit that drives the second solid state imaging device to obtain a second image signal;

a selection circuit that receives the first and second image signals to selectively output one of the received image signals in synchronization with time of operation of the first and second solid state imaging devices; and

an exposure control circuit that generates first and second exposure data, each of which indicates an amount of exposure for one of the first and second solid state imaging devices, so that a value of each of the first and second image signals output from the first and second solid state imaging devices falls within predetermined limits, wherein the exposure control circuit includes:

a first memory section that stores the first exposure data; and

a second memory section that stores the second exposure data.

10. An imaging unit according to claim 9, wherein the first and second solid state imaging devices operate in a time-division manner, and wherein, during a period when one of the first and second solid state imaging devices is operating, the exposure

control circuit successively updates a value of one of the first and second exposure data in accordance with an image signal obtained from the operating solid state imaging device, and holds a value of another one of the first and second exposure data without updating the value.

11. An imaging unit according to claim 10, wherein, when operation is switched between the first and second solid state imaging devices, the exposure control circuit uses, as an initial value to start operation, the value of the exposure data that is held during the period of suspension of operation.

12. An imaging unit according to claim 10, wherein, when operation is switched between the first and second solid state imaging devices, the exposure control circuit holds the values of the first and second exposure data input immediately before a time of switching of operation, for a predetermined period from the time of switching of operation.

13. An imaging unit, comprising:

a first solid state imaging device having a plurality of light receiving pixels that accumulate information charges generated in response to a first picture of a subject;

a first driving circuit that drives the first solid state imaging device to obtain a first image signal;

a second solid state imaging device having a plurality of

light receiving pixels that accumulate information charges generated in response to a second picture of the subject;

a second driving circuit that drives the second solid state imaging device to obtain a second image signal;

a selection circuit that receives the first and second image signals to selectively output one of the received image signals in synchronization with time of operation of the first and second solid state imaging devices; and

a white balance processing circuit that corrects white balance by applying predetermined gains to each of the first and second image signals, wherein the white balance processing circuit includes:

a first memory section that stores first gain data that indicates amount of gain to be applied to the first image signal; and

a second memory section that stores second gain data that indicates amount of gain to be applied to the second image signal.

14. An imaging unit according to claim 13, wherein the first and second solid state imaging devices operate in a time-division manner, and wherein, during a period when one of the first and second solid state imaging devices is operating, the white balance processing circuit successively updates a value of one of the first and second gain data in accordance with an image signal obtained from the operating solid state imaging device, and holds a value of another one of the first and second gain data without updating

the value.

15. An imaging unit according to claim 14, wherein, when operation is switched between the first and second solid state imaging devices, the white balance processing circuit uses, as an initial value to start operation, the value of the gain data that is held during the period of suspension of operation.

16. An imaging unit according to claim 14, wherein, when operation is switched between the first and second solid state imaging devices, the white balance processing circuit holds the values of the first and second gain data input immediately before a time of switching of operation, for a predetermined period from the time of switching of operation.